

Amendments to the Claims:

1-162. (canceled)

5 163. (currently amended) A chip ~~An electronic~~ package comprising:
a substrate comprising silicon;
a die joined with said substrate; and
~~an upper~~ a metallization structure over said die, wherein said ~~upper~~ metallization
structure comprises an electroplated metal.

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164. (currently amended) The ~~electronic chip~~ package in claim 163, wherein a cavity
[is] in said substrate [and] accommodates said die, said die having a bottom surface
joined with the bottom of said cavity.

15 165. (currently amended) The ~~electronic chip~~ package in claim 163, wherein said
substrate has a top surface comprising a first region and a second region, said die joined
with said first region, said second region not covered by said die, said first region being
substantially coplanar with said second region.

20 166. (currently amended) The ~~electronic chip~~ package in claim 163, wherein an
opening in said substrate accommodates said die, said substrate having a top surface
substantially coplanar with a top surface of said die and a bottom surface substantially
coplanar with a bottom surface of said die.

25 167. (currently amended) The ~~electronic chip~~ package in claim 163 further
comprising a polymer layer under a circuit ~~metal~~ layer of said ~~upper~~ metallization
structure.

168. (currently amended) The ~~electronic-chip~~ package in claim 163 further comprising a polymer ~~polymr~~-layer over a circuit ~~metal~~-layer of said ~~upper~~-metallization structure.

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169. (currently amended) The ~~electronic-chip~~ package in claim 163, wherein said die has a top surface at a horizontal level, said substrate being under said horizontal level, said ~~upper~~-metallization structure being over said horizontal level.

10 170. (currently amended) The ~~electronic-chip~~ package in claim 169, wherein said top surface comprises multiple pads.

171. (currently amended) The ~~electronic-chip~~ package in claim 169 further comprising a passive device over said horizontal level.

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172. (currently amended) The ~~electronic-chip~~ package in claim 163, wherein said ~~upper~~-metallization structure further extends across an edge of said die and to a place not over further extending outside beyond an edge of said die.

20 173. (currently amended) The ~~electronic-chip~~ package in claim 163 further comprising an adhesive tape joining said die and said substrate.

174. (currently amended) The ~~electronic-chip~~ package in claim 163 further comprising [an] a conductive paste joining said die and said substrate.

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175. (currently amended) The ~~electronic-chip~~ package in claim 163 further comprising a bump on a pad of said ~~upper~~-metallization structure, wherein said bump comprises solder.

176. (currently amended) The ~~electronic chip~~ package in claim 163 further comprising a bump on a pad of said ~~upper~~-metallization structure, wherein said bump comprises gold.

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177. (currently amended) The ~~electronic chip~~ package in claim 163 further comprising a film layer over said substrate and surrounding said die.

178. (currently amended) The ~~electronic chip~~ package in claim 177, wherein said
10 film layer comprises polymer.

179. (currently amended) ~~An electronic~~ A chip package comprising:
a substrate comprising silicon;
a die joined with said substrate ~~comprising multiple internal circuits~~; and
15 ~~an upper~~ a metallization structure over said die, wherein said ~~upper~~-metallization
structure comprises a metal trace portion connecting multiple separate pads of said die.
~~multiple internal circuits.~~

180. (currently amended) The ~~electronic chip~~ package in claim 179, wherein a cavity
20 [is] in said substrate [and] accommodates said die, said die having a bottom surface
joined with the bottom of said cavity.

181. (currently amended) The ~~electronic chip~~ package in claim 179, wherein said
substrate has a top surface comprising a first region and a second region, said die joined
25 with said first region, said second region not covered by said die, said first region being
substantially coplanar with said second region.

182. (currently amended) The ~~electronic chip~~ package in claim 179, wherein an

opening is in said substrate and accommodates said die, said substrate having a top surface substantially coplanar with a top surface of said die and a bottom surface substantially coplanar with a bottom surface of said die.

5 183. (currently amended) The ~~electronic chip~~ package in claim 179 further comprising a polymer layer under a circuit metal-layer of said ~~upper~~-metallization structure.

10 184. (currently amended) The ~~electronic chip~~ package in claim 179 further comprising a polymer layer over a circuit metal-layer of said ~~upper~~-metallization structure.

15 185. (currently amended) The ~~electronic chip~~ package in claim 179, wherein said metal trace portion-is used to transmit a signal.

 186. (currently amended) The ~~electronic chip~~ package in claim 179, wherein said metal trace portion-is used to provide a power voltage.

20 187. (currently amended) The ~~electronic chip~~ package in claim 179, wherein said metal trace portion-is used to provide a ground voltage.

 188. (currently amended) The ~~electronic chip~~ package in claim 179, wherein said die has a top surface at a horizontal level, said substrate being under said horizontal level, said ~~upper~~-metallization structure being over said horizontal level.

25 189. (currently amended) The ~~electronic chip~~ package in claim 188, wherein said top surface comprises multiple pads.

190. (currently amended) The ~~electronic-chip~~ package in claim 188 further comprising a passive device over said horizontal level.

191. (currently amended) The ~~electronic-chip~~ package in claim 179, wherein said
5 ~~upper~~-metallization structure further extends across an edge of said die and to a place not
over extending outside beyond an edge of said die.

192. (currently amended) The ~~electronic-chip~~ package in claim 179 further comprising an adhesive tape joining said die and said substrate.

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193. (currently amended) The ~~electronic-chip~~ package in claim 179 further comprising [an] a conductive paste joining said die and said substrate.

194. (currently amended) The ~~electronic-chip~~ package in claim 179 further
15 comprising a bump on a pad of said ~~upper~~-metallization structure, wherein said bump comprises solder.

195. (currently amended) The ~~electronic-chip~~ package in claim 179 further
20 comprising a bump on a pad of said ~~upper~~-metallization structure, wherein said bump comprises gold.

196. (currently amended) The ~~electronic-chip~~ package in claim 179 further comprising a film layer over sad substrate and surrounding said die.

25 197. (currently amended) ~~An electronic-~~A circuitry component comprising:
a die ~~having a top surface at a horizontal level, wherein said die comprises multiple~~
~~internal circuits; and~~
~~an upper~~-a metallization structure over said die and extending across an edge of said

die and to a place not over said die, horizontal level, wherein said ~~upper~~-metallization structure comprises a portion connecting said ~~multiple~~ separate pads of said die ~~internal~~-circuits and used to provide a ground voltage, ~~wherein said upper metallization structure extends outside beyond an edge of said die.~~

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198. (currently amended) The ~~electronic circuitry~~ component in claim 197 further comprising a substrate joined with said die.

10 199. (currently amended) The ~~electronic circuitry~~ component in claim 198, wherein said substrate comprises silicon.

200. (currently amended) The ~~electronic circuitry~~ component in claim 198, wherein a cavity [is] in said substrate [and] accommodates said die, said die having a bottom surface joined with the bottom of said cavity.

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201. (currently amended) The ~~electronic circuitry~~ component in claim 198, wherein said substrate has a top surface comprising a first region and a second region, said die joined with said first region, said second region not covered by said die, said first region being substantially coplanar with said second region.

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202. (currently amended) The ~~electronic circuitry~~ component in claim 197 further comprising a polymer layer under a circuit metal-layer of said ~~upper~~-metallization structure.

25 203. (currently amended) The ~~electronic circuitry~~ component in claim 197 further comprising a polymer layer over a circuit metal-layer of said ~~upper~~-metallization structure.

204. (currently amended) The ~~electronic circuitry~~ component in claim 197 further comprising a film layer surrounding said die and under said metallization structure, wherein ~~an opening is in said film layer and accommodate said die~~, said film layer having has a top surface substantially coplanar with [said] a top surface of said die and a bottom
5 surface substantially coplanar with a bottom surface of said die.

205. (currently amended) The ~~electronic circuitry~~ component in claim 204, wherein said film layer comprises polymer.

10 206. (currently amended) The ~~electronic circuitry~~ component in claim 197, wherein said portion comprises a ground bus.

207. (currently amended) The ~~electronic circuitry~~ component in claim 197, wherein said die has a top surface of said die comprises with multiple pads and at a horizontal
15 level, said metallization structure being over said horizontal level.

208. (currently amended) The ~~electronic circuitry~~ component in claim 207 [197] further comprising a passive device over said horizontal level.

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